MODEL AVR-32

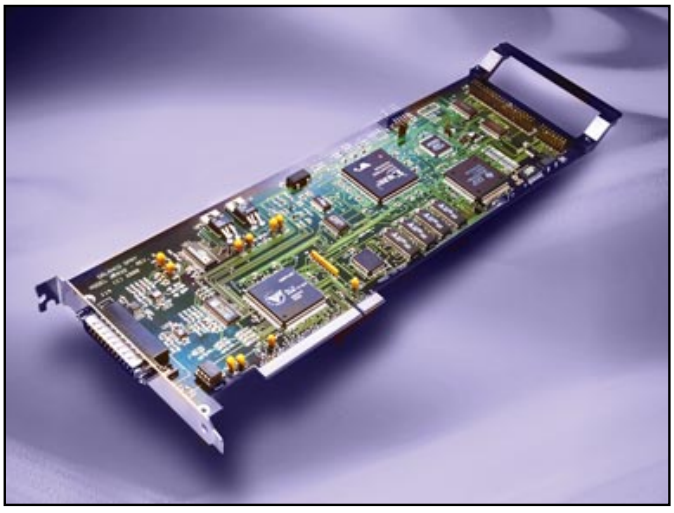
avr_32 < = power & flexibility;

OVERVIEW

The Model AVR-32 is a high performance signal processing and data acquisition board for the PCI Bus. Applications include Digital Signal Processing, Data Acquisition, Instrumentation, Control, and Embedded Systems. Processing power is provided by the Texas Instruments TMS320C32 DSP and Xilinx Virtex FPGA. High speed A/D and D/A converters and a digital data connector form the I/O section. The digital data connector may be configured as an IDE connector for direct-to-disk data acquisition and playback applications.

DESCRIPTION

The TI TMS320C32 is a 60 MHz floating point DSP with up to 60 MFLOPS performance. The Xilinx Virtex FPGA (Field Programmable Gate Array) is a high capacity, user reprogrammable logic device ideally suited for the implementation of many high speed DSP algorithms.The PCI-Local Bus bridge supports multiple modes of data transfer, whether initiated by the PC Host, the DSP, or the Virtex FPGA. A/D and D/A conversion are provided by high speed 12 bit devices.The Direct Digital Synthesizer (DDS) is used primarily for setting the A/D and D/A sampling rates. It may be programmed by the PC Host, the TMS320 DSP, or the Virtex FPGA.



FLEXIBILITY

Model AVR-32 functionality is flexible and is determined by the functions and datapaths programmed in the Virtex FPGA. Example configurations are:

- The Virtex FPGA serves as a conduit between the I/O section and the Local Bus in the default configuration. FIFO memories and interrupts are implemented to facilitate data throughput at high rates between the analog I/O and the Local Bus. The digital I/O is configured as an IDE connector.
- The Virtex FPGA is configured as a digital filter. A filter implemented in this manner can run at sample rates far in excess of an equivalent filter run on a DSP alone.
- The Virtex FPGA is configured as a specialized high speed processor with Local Bus mastering capability.

BOOT LOADER

The Boot Loader Mode of operation of the TMS320C32 is fully supported on the Model AVR-32. In this mode, the TMS320 DSP loads software and Virtex configuration data from Flash memory at power-up. The Model AVR-32 may thus operate independently of a PC Host.

SOFTWARE

Programs for the TMS320 DSP are created and debugged with the Dalanco Spry Assembler and Debugger included in the AVR-32 Software Development Kit. The TI C3x/C4x C Compiler and Assembler package may also be used. The TMS320C32 emulator port is available for use with development tools available from TI and other vendors.

Applications examples, including a data acquisition example, and device drivers for Windows 98/NT/2000 are included with the AVR-32 SDK, as are utilities for the Flash memory, the Virtex FPGA, and the DDS.

MODEL AVR-32
SPECIFICATIONS

Digital Signal Processor
60 MHz Texas Instruments TMS320C32 floating point DSP

Memory
512K Bytes 0 wait state SRAM
512K Bytes Flash memory

Field Programmable Gate Array
Xilinx Virtex FPGA
50K gate XCV50-6 is standard. May be substituted with larger (up to 800K gate), pin-compatible Virtex device

Analog Input
12 bit, 3 MSPS (or faster, pin-compatible) A/D converter, +/-2.5V input range

Analog Output
12 bit, 25+ MSPS D/A converter, +/-2.5V output range

Direct Digital Synthesizer (DDS)
Generates clock signal in the 0-20 MHz range with .015 Hz resolution

Digital I/O
High speed general purpose 16 bit I/O. May be configured as IDE connector for direct-to-disk data acquisition

Connectors
12 pin header for DSP emulation
DSP serial port connector
Auxiliary DIO connector

PCI Bus Interface
Master, slave, or DMA interface capable of sustained high data transfer rates
Interrupts
Mailbox registers

Physical
Full length PCI card

Warranty
1 year

For additional information please contact:

DALANCO SPRY
89 Winslow Avenue
Rochester, NY 14620
Tel:716-473-3610
Fax:716-271-8380
www.dalanco.com
sales@dalanco.com